REMARKS

This amendment is responsive to the Official Action dated March 27, 2004.

Claims 45-72 were pending in the application.

No claims were allowed.

No changes are made to the claims.

Accordingly, claims 45-72 are currently pending in the application.

By way of this amendment, the Applicant has amended the first paragraph of the Specification (Cross-reference to Related Applications) to update the claims of priority to earlier filed applications.

Brief Discussion of the Invention:

The claimed inventions in this application address a problem that can occur in the packaging of VCSELs and other surface normal optoelectronic devices and that has not been addressed in the prior art. One of the major advantages of VCSELs as lasers is the fact that they can be tested and characterized on-wafer to determine their suitability for packaging. This can be a great cost advantage.

Unfortunately, some packaging procedures, such as solid material encapsulation, change the device characteristics of typical VCSELs, making it difficult to predict the performance of packaged devices as compared to the on-wafer performance. The term encapsulation as used within the present specification is intended to mean a solid, optically transmissive encapsulation material that is molded over the VCSEL device and that surrounds the VCSEL device, imbedding the VCSEL device within the encapsulation material. The encapsulation material is in physical contact with the VCSEL device. The changes in the device characteristics that occur when encapsulated occur as a result of the interface between the surface of the VCSEL and the surface of the encapsulation material rather than air.

Continuing with the noted limitation that the device is encapsulated, a question then arises. Can the devices be fabricated in such a way as to make the on-wafer performance the same as the packaged (encapsulated) performance? This application presents a totally non-

obvious affirmative answer to that question. *Surprisingly, the deposition of a pre-calculated thickness of just one extra layer of optically transparent material, atop the VCSEL, can adjust the reflectivity of the top VCSEL mirror, so as to make the on-wafer performance the same as the packaged performance.*

Objection to Drawing Figures:

The Examiner has objected to the drawings, and has requested new drawing figures.

Applicant will submit new FORMAL drawings upon the indication of allowable subject matter.

Applicant's previous arguments with respect to claims 45-72 were considered but are moot in view of the NEW grounds of rejection.

However, the majority of those arguments are still relevant and applicable to a discussion of the newly cited reference (Davis). Those previous arguments are incorporated herein by reference. The previous arguments are also repeated in the attached addendum.

Claim Rejections under 35 USC §103 (Davis):

Claims 45-72 were rejected under 35 USC §103 as being unpatentable over Davis et al USP 6069905.

The Applicant submits that the cited Davis et al. patent (US patent 6,069,905) has no bearing at all on the present application for two principal reasons:

-- a) the implementations of the inventions in the cited patent and in the present application are completely different, and

-- b) the purpose and/or function of the inventions in the cited patent and in the present application are completely different. Explanations follow.

Re (a). - The first principal invention in this application is the medium-matching layer. It is deposited directly onto the top surface of an active optical device (the top emitting surface of the top mirror, in the case of a VCSEL). This deposition is done when the devices are still in wafer form, so it is done typically to thousands of devices simultaneously, prior to "on wafer" testing and characterization and long before the devices are diced apart, packaged,

and encapsulated. In Davis et al. (US patent 6,069,905), according to its Figure (3), the layer, 37, is deposited onto the tilted window, 37, of a can package, 34, and not onto the device (VCSEL), 10. Also, the inventions in Davis et al. (US patent 6,069,905) are all packaging issues done with one VCSEL at a time. *Another important point needs to be made at this point. When we speak of encapsulation, in this application, we do not mean packaging. Encapsulation is one particular step in packaging. In the Figure (3) in Davis et al. (US patent 6,069,905), if encapsulation was to be done, it would involve filling the region (or void), between the devices (10&14) and the can package, 34 (with its tilted window, 37), with some material, whose index of refraction is substantially greater than 1, other than air, vacuum, or any gas, whose indices of refraction are approximately equal to 1. One possible reason for encapsulation is hermetic sealing, with an epoxy for instance. Another reason is to prevent reflections back into active devices from a surface of a passive component in the package, with a gel for instance, whose index of refraction matches that of the passive component. In many optical assemblies, there is no need for encapsulation and so it is not done.* ***There is no mention of encapsulation in Davis et al. (US patent 6,069,905).*** *Although the medium-matching layer is the first principal invention in this application, its usefulness only becomes truly apparent, when an active device is placed in an optical assembly and is encapsulated. That is the reason the claims in this application are structured as they are.* How and why the medium-matching layer does what it does was explained in the descriptive section of the application and is again explained in the addendum to this official action.

The second principal invention in this application is the combination of a tuning layer and a medium-matching layer in tandem. The tuning layer is placed just under the medium-matching layer. All the above explanations for the implementation of the medium-matching layer alone, apply to the tandem pair verbatim.

Re (b). The function of the medium-matching layer, in this application, is to allow an optoelectronic device, such as a VCSEL, to exhibit the same characteristics, whether it is in air, where the index of refraction, n_a, is approximately equal to 1, or in another medium, such as an epoxy or a gel, where the index of refraction is some other given value, n_m. How and why the medium-matching layer does this was explained in the descriptive section of the

application and is again repeated in the addendum to this response. (Note, that for each different value of n_m a different medium-matching layer is needed.) One example of the usefulness and thereby the purpose of this function is better explained with the aid of the attached Figure 1. The figure shows two hypothetical L-I (light output, L, versus bias current, I) curves for a VCSEL. The two curves (solid and dashed, respectively) have different threshold currents, I_{th} (a) and I_{th} (b), and different slope efficiencies, η_a and η_b. Without a medium-matching layer, the same VCSEL will exhibit such two different L-I curves, such as the dashed when the medium is air, with an index n_a, ~1, and such as the solid when the medium has an index n_m, > 1. *On the other hand, with a medium-matching layer, the VCSEL will have the same L-I curve, i.e. the same I_{th} and the same η, whether it is in air or the other medium.* That means the VCSEL will have the same L-I curve, once in a package and encapsulated, as it did at wafer level testing. This can be a huge cost-saving advantage in the assembly of VCSEL modules.

Generally, a VCSEL module must meet certain requirements or specifications. Among these, for example, is a specification on the average optical output power, L_{ave}, and upon modulation, on either the difference or the ratio of the optical output powers L_{hi} and L_{lo} (for a high signal, binary 1, and a low signal, binary 0, respectively). To achieve such specifications the drive circuits in the module must deliver a constant bias current, I_{ave}, for the average power, L_{ave}, and a modulation current, I_{mod}, to modulate the VCSEL between the powers L_{hi} and L_{lo}. Foreknowledge, of the VCSEL L-I curve, produces cost-savings in at least three ways. It allows one to avoid packaging unsatisfactory VCSELs, it allows the use of cheaper drive circuits, with less range and sophistication, and it simplifies the setting of I_{ave} and I_{mod}. The use of the tandem pair of layers, tuning and medium-matching, gives all the above advantages and in addition the possibility of turning thousands of VCSELs, simultaneously at wafer level, from unsatisfactory into satisfactory ones, by tuning their L-I curves.

The inventions in Davis et al. (US patent 6,069,905) do not accomplish any of above. However, they do accomplish something different and also very important, which our application does not address. Davis provides a feedback loop, which allows a module to

automatically adjust IL_{ave} so as to maintain the same L_{ave}. The purposes of the inventions in the present application and in Davis et al. (US patent 6,069,905) are mutually orthogonal.

For the above reasons, it is submitted that the cited patent, Davis et al. (US patent 6,069,905), contains no teaching or suggestion that would render any of the claims in our application as obvious.

Withdrawal of the Section 103 rejection in view of Davis et al, and review and reconsideration of claims 45-72 is respectfully solicited.

Claim Rejections under 35 USC §103 (Scott and Swirhun):

Claims 45-72 were rejected under 35 USC §103 as being unpatentable over Scott et al (USP 6,567,435) in view of Swirhun (USP 5,577,064).

The US Patent to Scott USP 6,567,435 is claimed as a parent application in the present application. The Examiner is invited to refer back to the Amendment filed February 7, 2003 in which the Applicant filed a substitute specification identifying the Scott et al specification as a parent application (US Patent Application No. 09/531,442). The details of the serial number of the '435 application filed March 20, 2000, were initially omitted from the present specification due to proximity of the filing dates. However, these details were later included in the substitute specification filed February 7, 2003.

The first paragraph of the specification has now been amended to update the issued status of the Scott patent.

Accordingly, the rejection of claims 45-72 in view of the Scott reference is believed to be moot in view of the claim of priority. Withdrawal of the rejection and reconsideration of claims 45-72 is respectfully solicited.

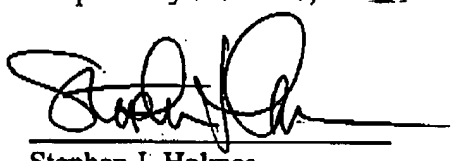
Claims 45-72 are thus believed to be in condition for allowance and the application now ready for issue.

Corresponding action is respectfully solicited.

Serial No. 09/535,629

PTO is authorized to charge any additional fees incurred as a result of the filing hereof or credit any overpayment to our account #02-0900.

Respectfully submitted,



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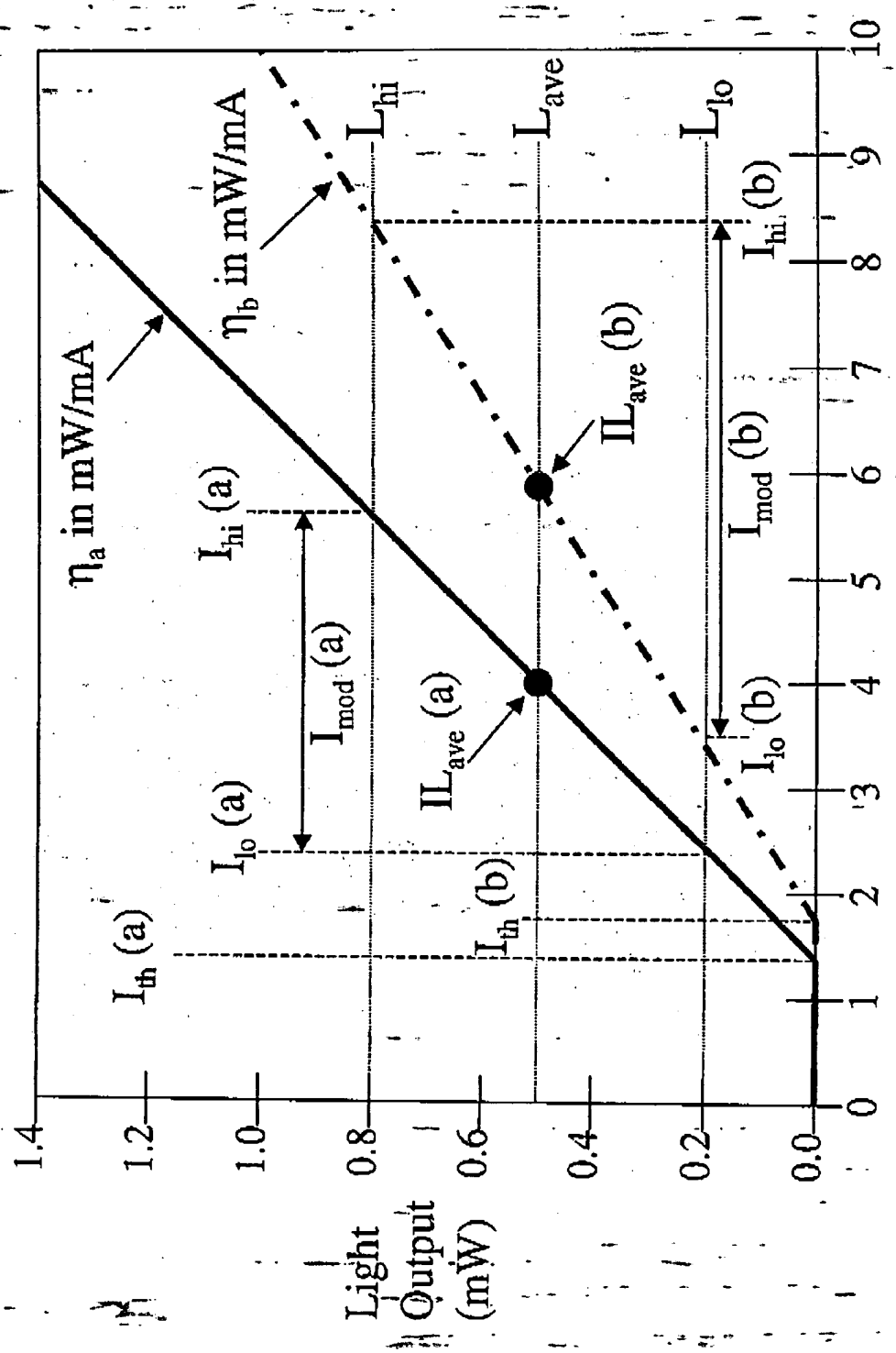


FIGURE 1. Hypothetical VCSEL L-I Curves

ADDENDUM

The claimed inventions in this application address a problem that can occur in the packaging of VCSELs that has not been addressed in the prior art, including Davis et al. (US patent 6,069,905). One of the major advantages of VCSELs as lasers is the fact that they can be tested and characterized on-wafer to determine their suitability for packaging. This can be a great cost advantage. **Unfortunately, some packaging procedures, such as encapsulation, necessarily change the device characteristics of typical VCSELs, making it difficult to predict the performance of packaged devices from the on-wafer performance.** A question then arises. Can the devices be fabricated in such a way as to make the on-wafer performance the same as the packaged performance? **This application presents a totally not obvious affirmative answer to that question.** *Surprisingly, the deposition of a pre-calculated thickness of just one extra layer of optically transparent material, atop the VCSEL, can adjust the reflectivity of the top VCSEL mirror, so as to make the on-wafer performance the same as the packaged performance.* We call this layer the medium-matching layer. Then, a second important question arises. Can the devices be fabricated in such a way as to not only make the on-wafer performance the same as the packaged performance, but to make both conform to tight predetermined specifications? **Once again, this application presents a totally not obvious affirmative answer.** *The deposition of a pre-calculated thickness of two different extra layers of optically transparent materials, atop the VCSEL, can adjust the reflectivity of the top VCSEL mirror; so as to make the on-wafer performance the same as the packaged performance, with both conforming to tight predetermined specifications.* Below is a detailed explanation of how the medium-matching layer functions and then how that medium-matching layer functions with a tuning layer just under it.

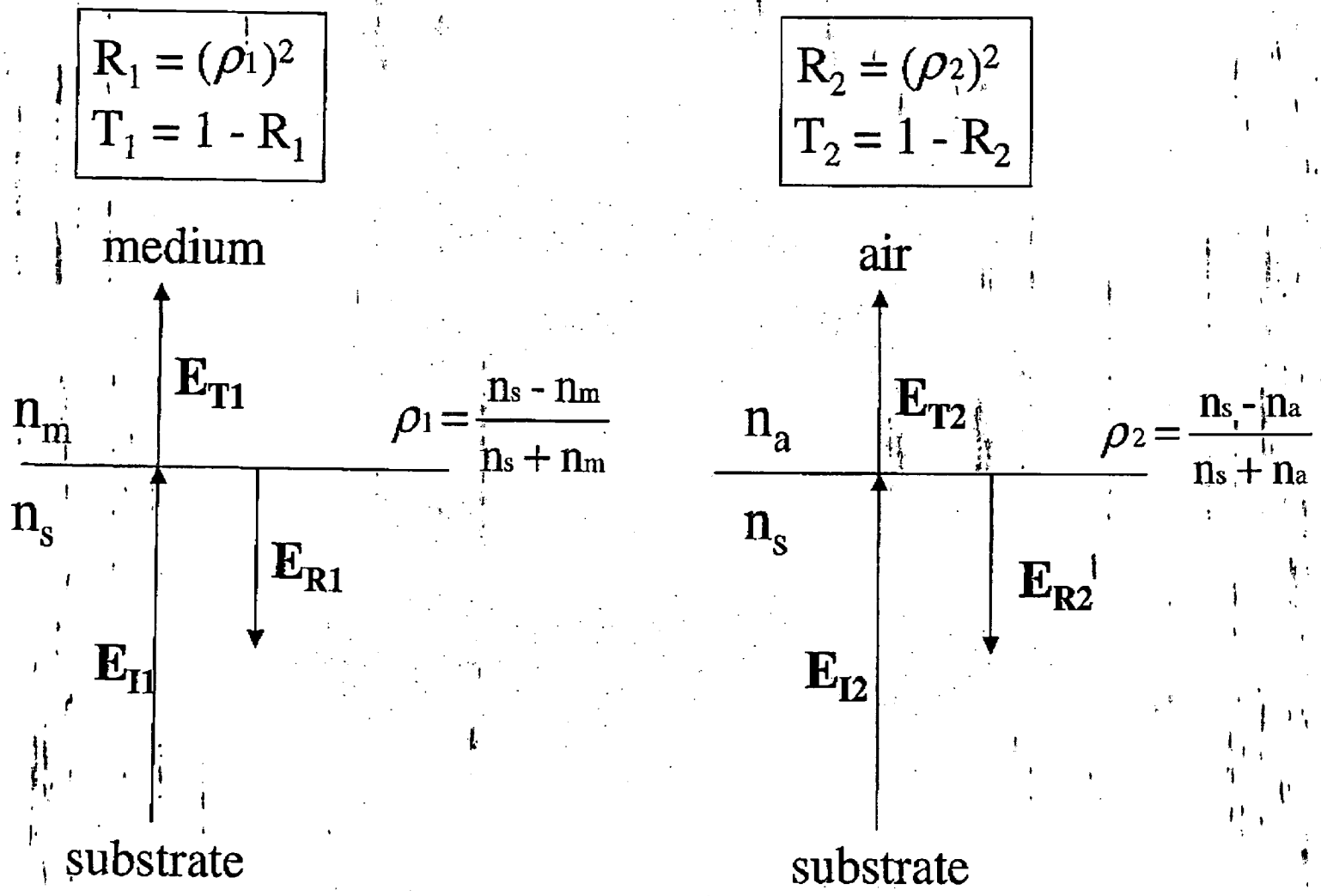
VCSEL mirrors are Distributed Bragg Reflectors (DBR's), consisting of alternating layers of materials with different indices of refraction, with each layer a quarter-wave thick. Each interface, where the index changes, partially reflects an incident beam by an amount given by the equation, $R = (n_1 - n_2)^2 / (n_1 + n_2)^2$. The quarter-wave thickness of each layer is a phase-matching thickness, causing all the partial reflections to enjoy completely constructive interference, maximizing the reflectivity for the given number of interfaces. The last interface

is between the last mirror layer and the medium into which the VCSEL launches light, which is usually air with an index of refraction ≅ 1 (it is air during on-wafer testing). This last interface always makes a significant contribution to the total reflectivity of the top mirror. The reflectivity of the last interface depends only on the index of the last mirror layer and on the index of the medium, although the medium is not per se a part of the VCSEL structure. It does not depend on what is beneath the last layer, so for simplicity of discussion one can analyze the situation while having no other layers or interfaces below the last interface, making it the only interface between a substrate (with an index, n_s) and a medium (with an index, n_m) as is shown in Figure A1. If one changes the medium, as one does by encapsulating a device, then one necessarily changes the reflectivity of the last interface (as is shown in Figure A1), and in a VCSEL, one thereby changes the total reflectivity of a top mirror and so changes the device performance. This result appears to be inescapable.

The first primary invention (the medium-matching layer) described in our application, and again illustrated in the attached Figure A2, first of all recognizes that the last mirror layer (or equivalently the substrate in Figure A2) can be covered by an additional layer to create two last interfaces, whose reflectivities need to be analyzed in tandem. The reflectivity of that pair of interfaces is a function of the reflectivities of each interface and of the phase angle between them, given by "k*d" (where d is thickness of the additional layer, and k is defined in Figure A2). The exact relationship is shown in Figure A3. At first sight, it appears that this is no solution. As the medium (that is the index of the medium) is changed, although the reflectivity of the lower interface does not change, the reflectivity of the upper interface does change, and to compensate for that change so as to keep the reflectivity of the tandem the same, it appears that one needs to change the phase angle, that is to change the thickness, d, of the additional layer, or its index (to change k). The second significant, unexpected insight in our application and the core of the first primary invention, is that for layers with a certain k, one can find a thickness, d, and thus a single phase angle "k*d", which yields the same reflectivity for the tandem of two interfaces, for two different mediums. Thus, for instance, such a "medium-matching" layer can yield the same reflectivity whether the medium is air, with an index, $n_a \cong 1$, or any encapsulant, with an index n_m. Most noteworthy is the fact that,

in practice, this "medium-matching" layer can be and should be deposited during wafer-level device fabrication prior to on-wafer testing. Thus, all the devices on the wafer will already have the same characteristics during the on-wafer testing, as they will after they are packaged with an encapsulation. **The "medium-matching" layer is not deposited or attached during the packaging procedure because by then it is too late, since the on-wafer testing was completed beforehand.**

Even though the "medium-matching" layer yields the same reflectivity and thus the same performance for a device in two different mediums, it may not yield the "desired" reflectivity and performance. *The second important invention in this application is that a tuning layer can be placed between the last mirror layer and the "medium-matching" layer, so as to adjust the reflectivity to a particular value, which remains the same in two different mediums.* Scott et al (US patent 6,392,256) and a patent application cited therein ("Vertical Cavity Surface Emitting Lasers with Consistent Slope Efficiencies", Application # 09/237,580) disclose the use of a tuning layer, but only with it alone deposited on the last layer of the top mirror of a VCSEL, as shown in the attached Figure A4. Since the "medium-matching" layer and the tuning layer affect each other and each other's function, it is not obvious that they can be effectively combined. Also it is not obvious that their designs need to be different when combined than when separately deployed.



NOTE: $R_1 \neq R_2$ & $T_1 \neq T_2$, because $n_m \neq n_a$

Figure 1A. Elementary Example of the Problem

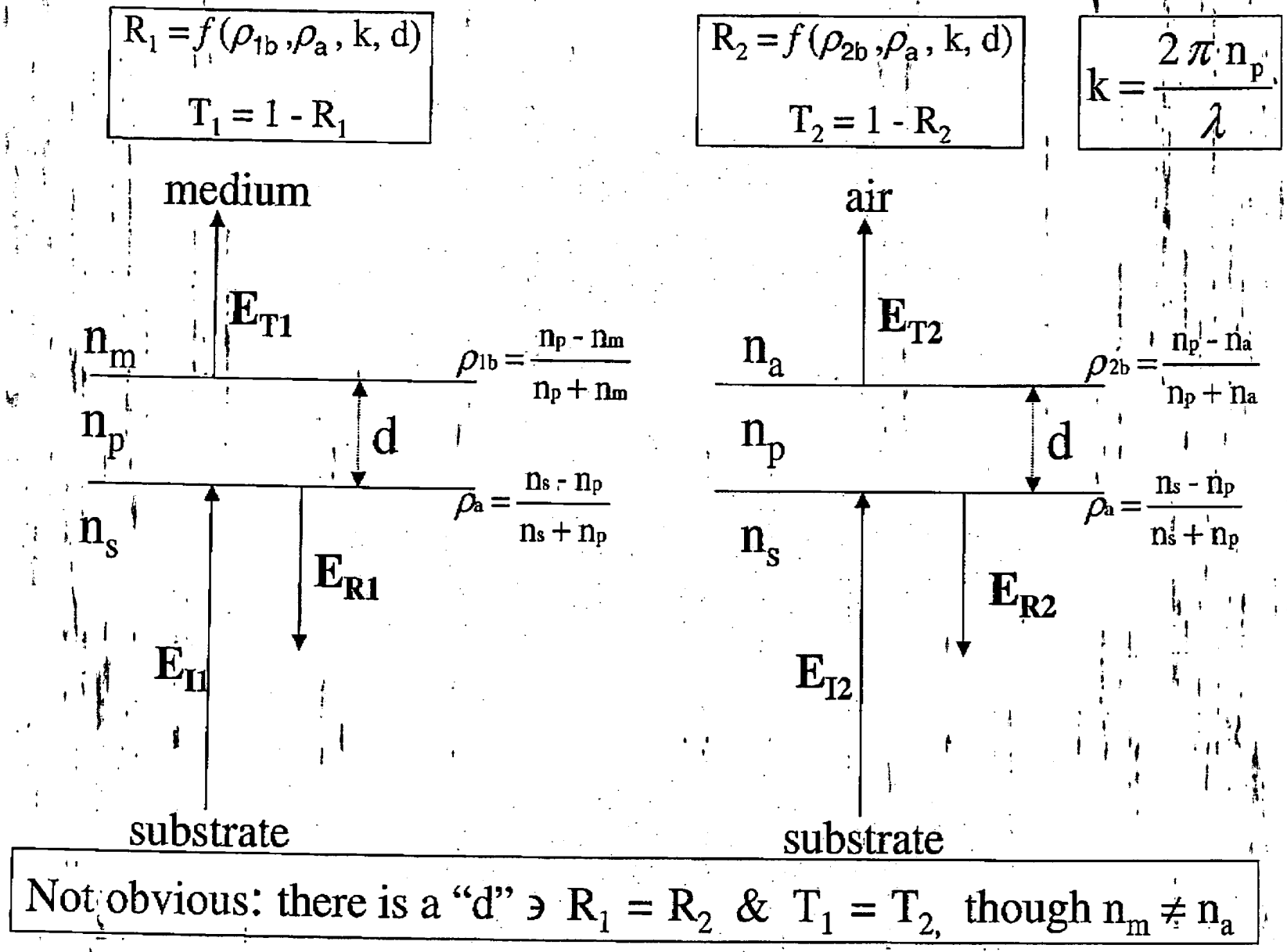


Figure 2A. Elementary Example of the Solution

$$R_1 = \frac{(\rho_a + \rho_{1b})^2 - 4\rho_a\rho_{1b}\sin^2 kd}{(1+\rho_a\rho_{1b})^2 - 4\rho_a\rho_{1b}\sin^2 kd}$$

$$R_2 = \frac{(\rho_a + \rho_{2b})^2 - 4\rho_a\rho_{2b}\sin^2 kd}{(1+\rho_a\rho_{2b})^2 - 4\rho_a\rho_{2b}\sin^2 kd}$$

Figure 3A. Formulas for the R1 & R2 in figure 2A

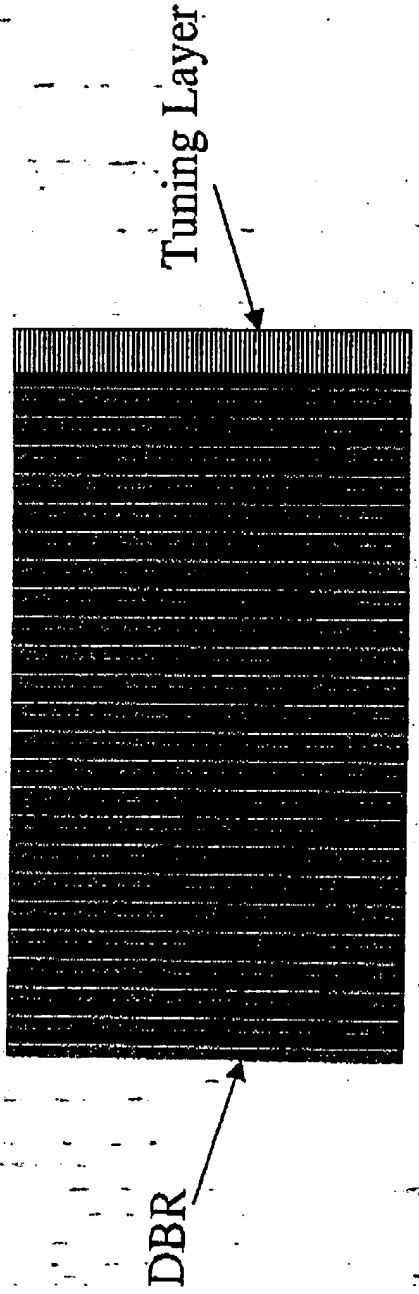


Figure 4A. Prior Art Tuning Layer